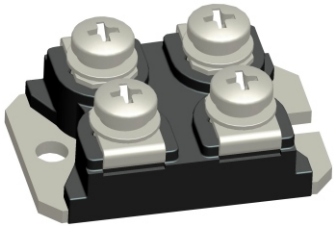
Back to Back SCR Module, 70A

FEATURES

- International standard package BLOC, ISOTOP compatible
- 2500V_{RMS} isolating voltage
- High surge capability
- **MESA SCR chips**
- International standard package mini BLOCK, ISOTOP compatible
- Compliant to RoHS
- Designed and qualified for multiple level

RoHS COMPLIANT



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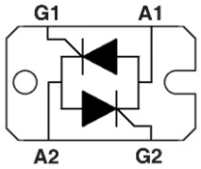
APPLICATIONS

- Solid state relays
- Welding equipment
- Light control
- Power converters
- Heat and temperature control
- Motor control circuits

Circuit Configuration :



PRODUCT SUMMARY	
$I_{T(RMS)}$	70A

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNIT
$I_{T(RMS)}$	85°C	70	A
I_{TSM}/I_{FSM}	50 Hz	700	
	60 Hz	735	
I^2t	50 Hz	2450	A^2s
	60 Hz	2242	
$I^2\sqrt{t}$		24500	$A^2\sqrt{s}$
V_{DRM}/V_{RRM}	Range	800 to 1600	V
T_J	Range	-40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{RRM}/V_{DRM}, MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM}/V_{DSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} AT 125 °C mA
NST70KQ	08	800	900	10
	12	1200	1300	
	16	1600	1700	

FORWARD CONDUCTION						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**			**VALUES**	**UNIT**
Maximum RMS on-state current	$I_{T(RMS)}$	180° conduction, half sine wave, 50Hz, T_C = 85°C			70	A
Maximum peak, one-cycle , on-state non-reptitive surge current	I_{TSM}	t = 10ms	No voltage reapplied	Sine half wave, initial T_J = T_J maximum	700	A
		t = 8.3ms			735	
		t = 10ms	100%V_{RRM} reapplied		588	
		t = 8.3ms			617	
Maximum I^2t for fusing	I^2t	t = 10ms	No voltage reapplied		2450	A^2s
		t = 8.3ms			2242	
		t = 10ms	100%V_{RRM} reapplied		1730	
		t = 8.3ms			1580	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			24500	$A^2\sqrt{s}$
Maximum on-state voltage drop	V_{TM}	I_{TM} = 100A, T_J = 25°C, 180° conduction			1.8	V
Maximum holding current	I_H	I_T = 0.5A			150	mA
Maximum latching current	I_L	I_G = 1.2 I_{GT}			400	

BLOCKING				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNIT**
Maximum peak reverse and off-state leakage current	I_{RRM} I_{DRM}	T_J = 125°C	10	mA
RMS isolation Voltage	V_{ISO}	50 Hz, circuit to base, all terminals shorted	2500 (1 min) 3000 (1 s)	V
Minimum critical rate of rise of off-state voltage	dV/dt	T_J = T_J maximum, exponential to 67% rated V_{DRM}	1000	V/μs

TRIGGERING					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**VALUES**	**UNIT**
Maximum peak gate power	P_{GM}	t_p ≤ 5 ms, T_J = T_J maximum		10	W
Maximum average gate power	$P_{G(AV)}$	f = 50 Hz, T_J = T_J maximum		3	
Maximum peak gate current	I_{GM}	t_p ≤ 5 ms, T_J = T_J maximum		3	A
Maximum peak negative gate voltage	$-V_{GT}$			10	V
Maximum required DC gate voltage to trigger	V_{GT}	T_J = 25°C	Anode supply = 12V, resistive load; R_L = 33Ω	1.3	
Maximum required DC gate current to trigger	I_{GT}			100	mA
Maximum gate voltage that will not trigger	V_{GD}	T_J = T_J maximum, 66.7% V_{DRM} = applied		0.25	V
Maximum gate current that will not trigger	I_{GD}			5	mA
Maximum rate of rise of turned-on current	dI/dt	T_J = 25°C, I_G = 2 x I_{GT}		150	A/μs

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNIT**
Maximum junction operating temperature range	T_J		-40 to 125	°C
Maximum storage temperature range	T_{stg}		-40 to 150	
Maximum thermal resistance, junction to case per junction	R_{thJC}	DC operation	0.45	°C/W
Maximum thermal resistance, case to heatsink per module	R_{thCS}	Mounting surface, smooth, flat and greased	0.10	
Mounting torque, ±10% — module to heatsink, M4 / busbar, M4		A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound. Lubricated threads.	1.1	N·m
Approximate weight			30	g
			1.06	oz.
Case style		JEDEC	SOT-227	

Ordering Information Table

Device code

N	ST	70	KQ	12
1	2	3	4	5

1 - Nell high Power Module
2 - Package indicator (SOT-227)
3 - Current rating, 70 for $I_{T(RMS)}$ = 70A
4 - Circuit configuration type
5 - Voltage code x 100 = V_{DRM}/V_{RRM}

Fig.1 RMS current vs. case temperature

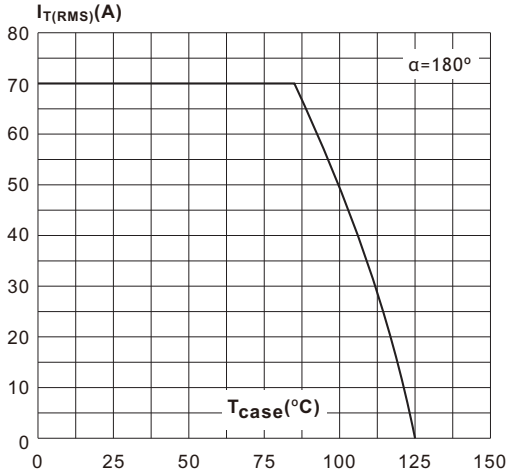


Fig.2 Transient thermal Impedance vs. time (per thyristor)

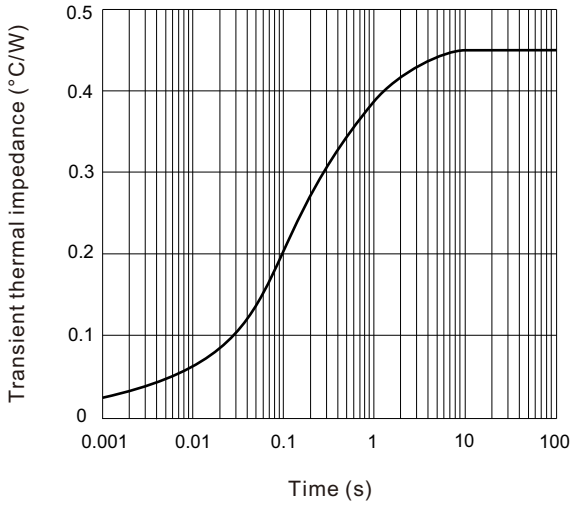


Fig.3 Power Dissipation vs. RMS Current

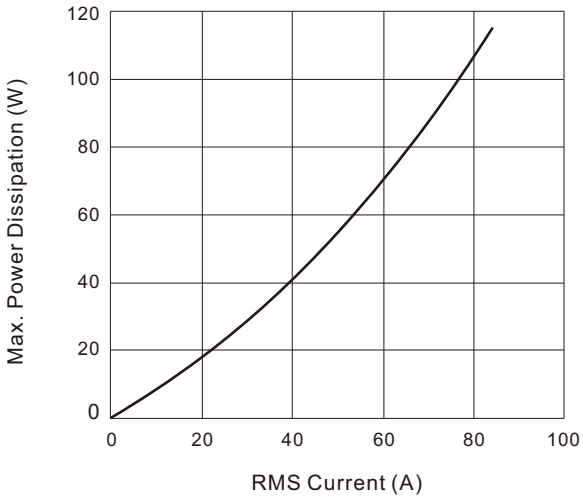


Fig.4 Surge On-state Current vs. Cycles

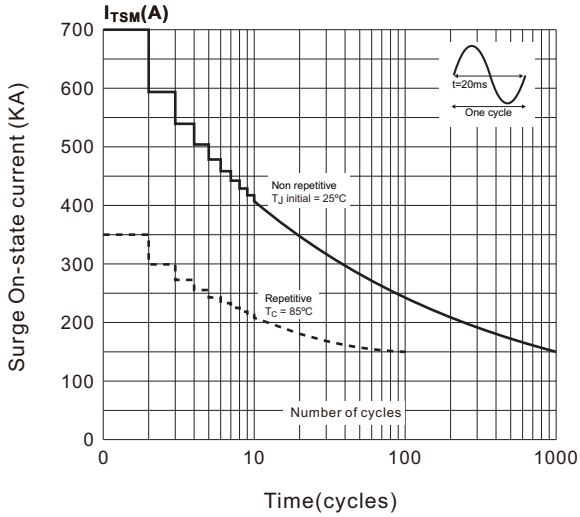


Fig.5 On- state characteristics (per thyristor)

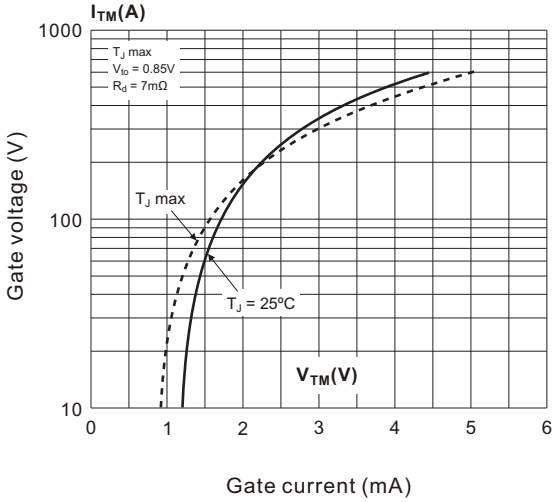


Fig.6 Relative variation of gate trigger current and holding current vs. junction temperature

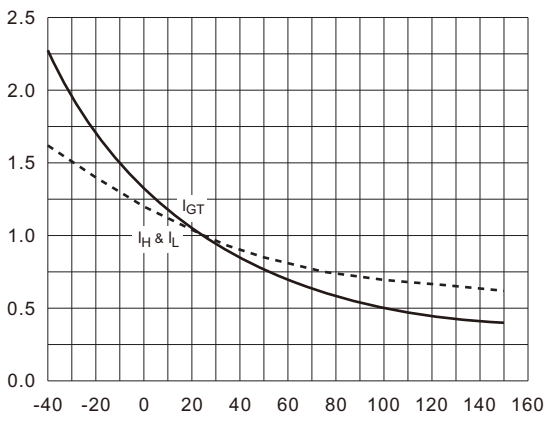
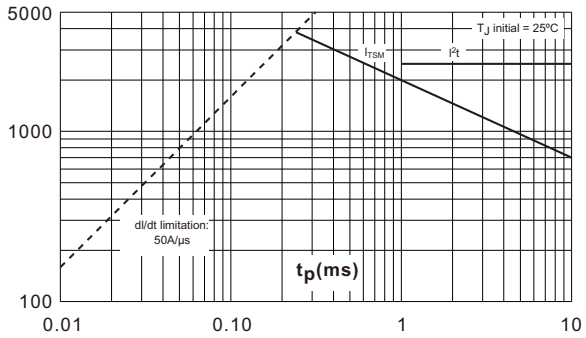


Fig.7 Non- repetitive surge peak on-state current, and corresponding values of I^2t



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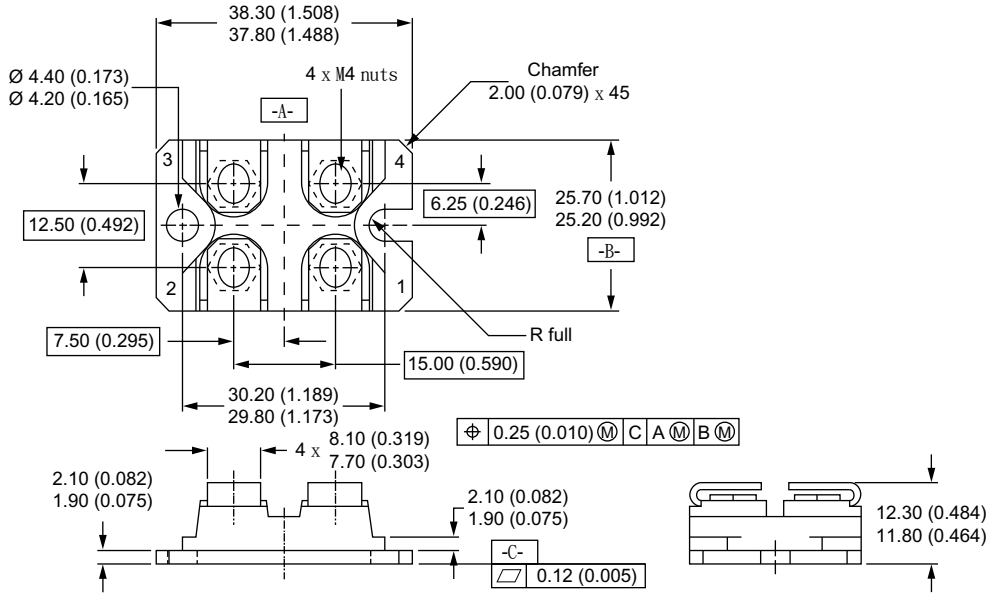

All dimensions in millimeters (inches)

Notes

- Dimensioning and toleranc ing per ANSI Y14.5M-1982
- Controlling dime nsion: millimeter